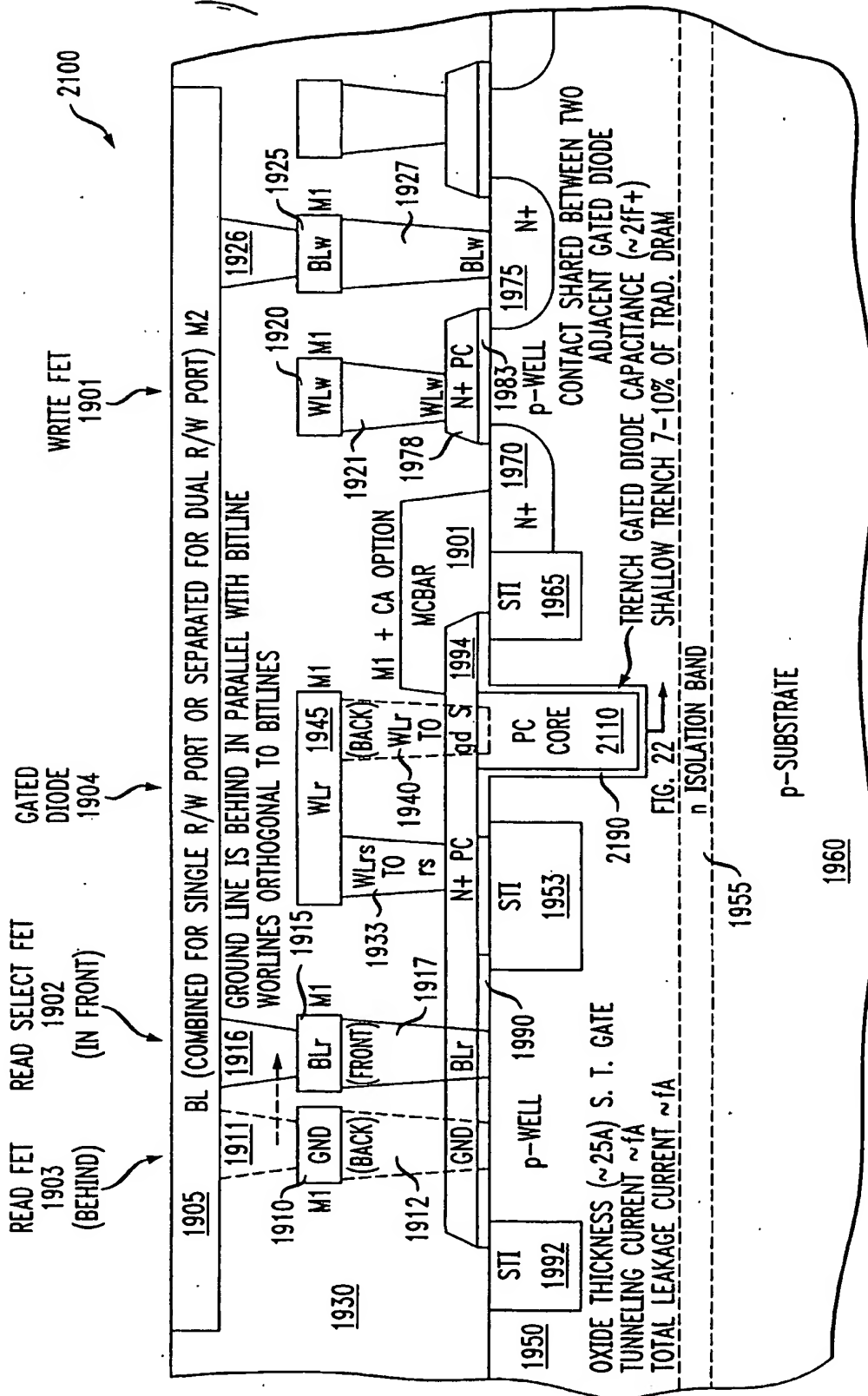


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FIG. 21



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FIG. 25

The diagram illustrates a 3T1D memory array architecture. It features a grid of wordlines (WL) and bitlines (BL). Wordline drivers are shown at the top, connected to wordlines labeled 2320-1A, 2320-1B, ..., 2320-NA, 2320-NB. Bitlines are labeled 2330-1, 2330-2, ..., 2330-M, 2330-N. The array contains 3T1D memory cells, each consisting of a transistor (T1) and a diode (D). The cells are connected to wordlines and bitlines. A note indicates that GND is shared by n bits, with an example of 8-16 BLr. The output of the array is connected to a series of inverters (2360-1, 2360-2, ..., 2360-M, 2360-N) which produce the final output signals (Dout, SA, BLPC, Din). The output signals are labeled BIT 0, BIT 1, ..., BIT j, BIT j+1, ..., BIT M-2, BIT M-1.

